Nepal College of Information Technology

**Unit Test**

Fall 2012

Program : BE CE/ELX Time : 2 hrs

Semester : (V) FM : 70

Subject : Integrated Digital Electronics PM : 35

* *Candidates are requested to give their answer as far as practicable in their own words.*
* *The figure in the margin indicates the full marks*
* ***Attempt ALL question***

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| **1.** | **a.** | Explain in detail, how the circuit shown below works as a logic inverter. Assuming =70, VBE (on) = 0.65V, VBE (sat) = 0.75V,VC E (sat) = 0.2 V, explain in detail and plot its VTC. | 2+6 |
|  | **b.** | Explain why IIL has high packing density. Draw 2-bit IIL decoder. | **2+5** |
| **2.** | **a.** | Stating all necessary assumptions you make, answer the following questions referring the following circuit. |  |
|  |  | 1. Explain how the circuit enclosed in dotted line (Go) works as a NAND gate. 2. Calculate the potential at point P and B when the output transistor (To) of the driving gate is in saturation. 3. Calculate the current flowing through the base resistor Rb when the input(Vi) is low and when the input(Vi) is high.(assume no inputs are applied to DB and DC diodes) 4. What is the role of base resistor Rb and the negative supply in the circuit above? 5. Derive an expression for the fan-out(N) for the Discrete Circuit DTL NAND gate Go. | 2  2  2  2  7 |
| **3.** | **a.** | Draw the input-output characteristics of RTL NOR gate for a fan-out of N=5 at  25 °C.  **OR**  Define fan-out. Calculate the fan out for the medium power standard RTL NOR gate. | 8 |
|  | **b.** | Draw an Exclusive-OR circuit using RTL and explain its operation.  **OR**  Draw the RTL buffer gate and explain how fan-out is improved in it ,in comparison to ordinary RTL gate. | 7 |
| **4.** | **a.** | Define noise margin. Calculate ∆0 and ∆1 noise margins for the ordinary RTL NOR gate at temperature 125 °C, without ignoring the temperature dependency of VCE (sat) . Assume, temperature sensitivity of base emitter junction is - 2 mV/°C. | 5 |
| **5.** |  | Write short notes on **(*Any Two*)**   1. Current Hogging in DCTL 2. 2-input RTL NOR gate 3. Physical layout of IIL 4. Propragation delay hazards | 2×5 |